

HD74LS48

BCD-to-Seven-Segment Decoder / Driver (Internal Pull-up outputs)

REJ03D0411-0300

Rev.3.00

Jul.22.2005

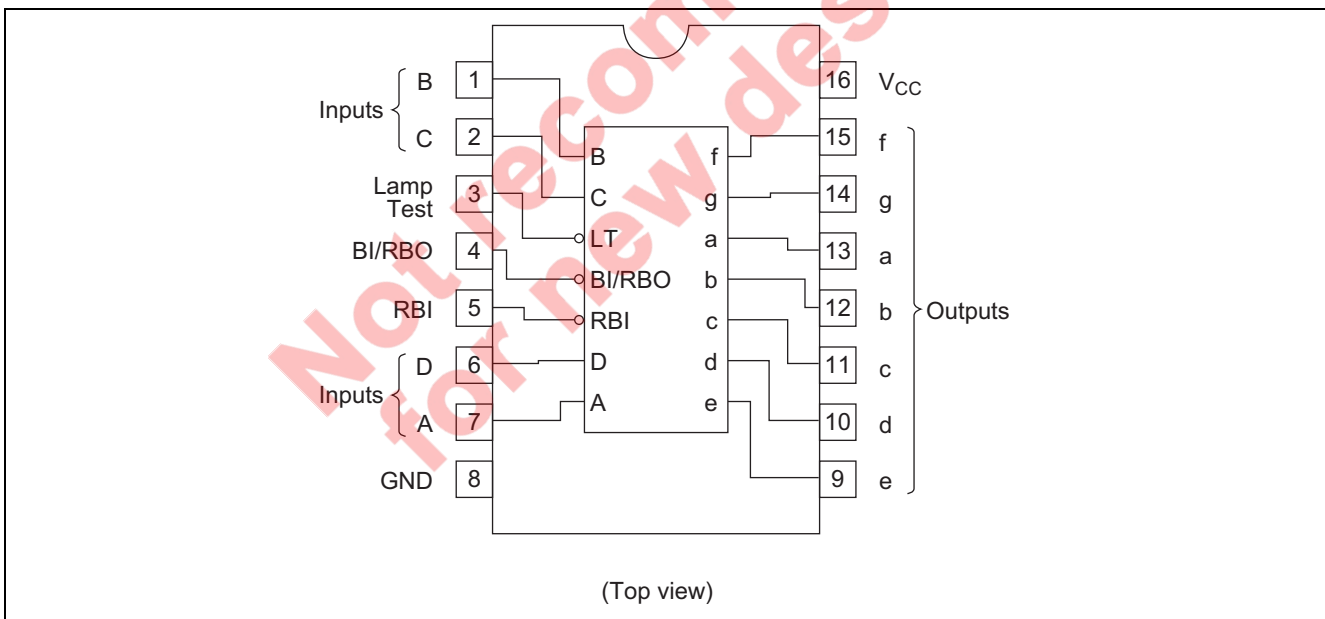
HD74LS48 features active high outputs for driving lamp buffers. This circuit has full ripple blanking input / output controls and a lamp test input. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions. This circuit incorporates automatic leading and / or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI / RBO node is at a high level. It contains an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Features

- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|-----------|--------------|------------------------------|----------------------|--------------------------------|
| HD74LS48P | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |

Pin Arrangement

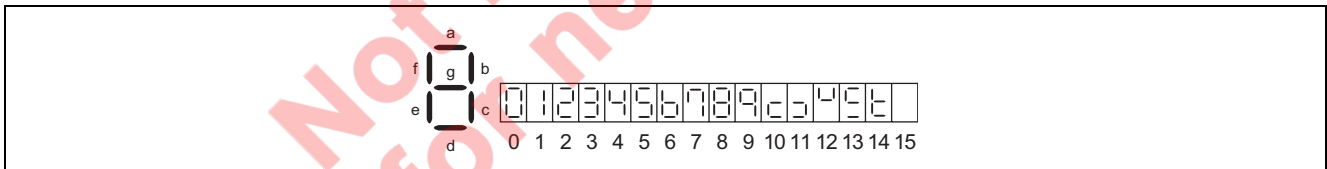


Function Table

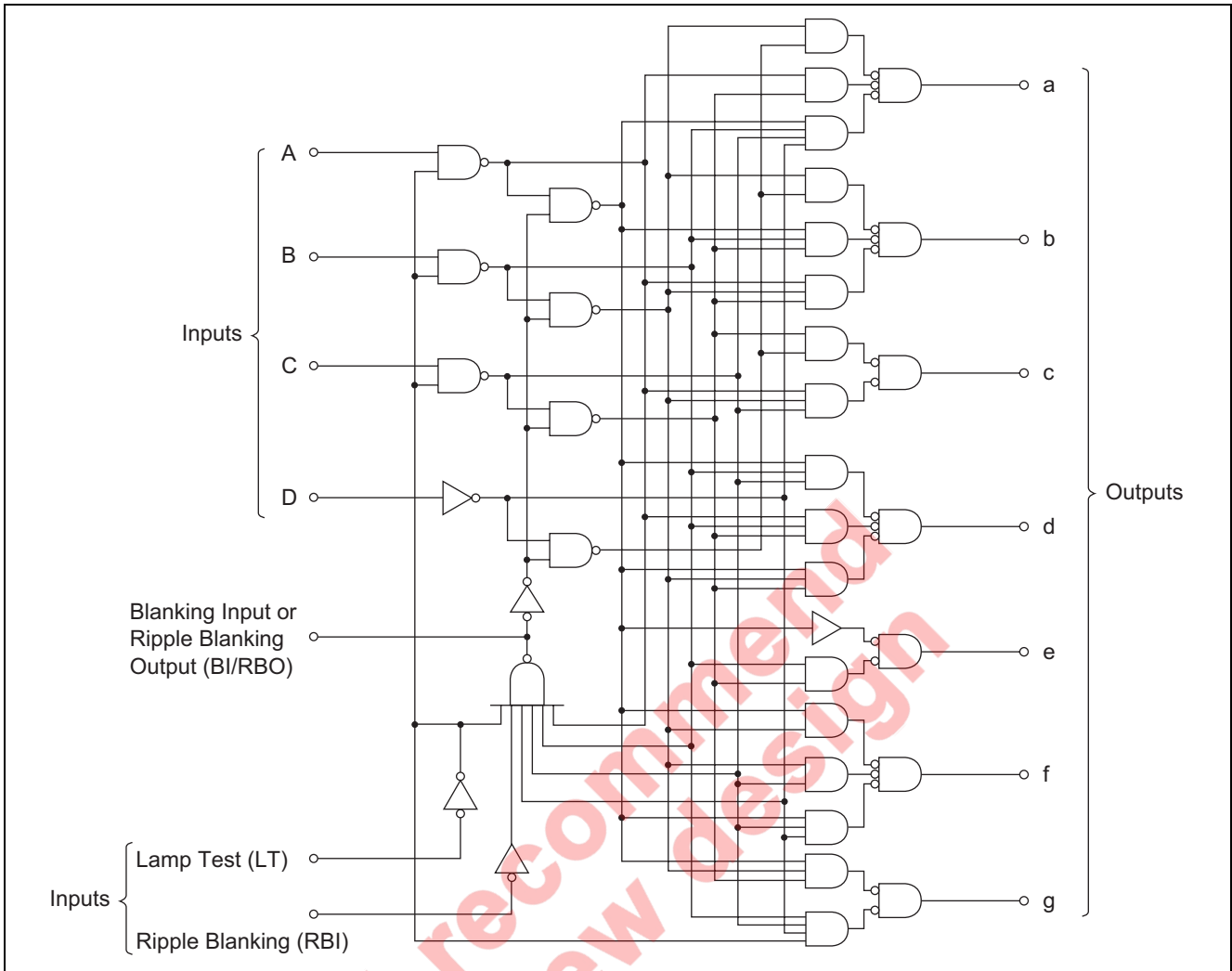
| Decimal or Function | Inputs | | | | | | BI / RBO | Outputs | | | | | | | Note |
|---------------------|--------|-----|---|---|---|---|----------|---------|---|---|---|---|---|---|------|
| | LT | RBI | D | C | B | A | | a | b | c | d | e | f | g | |
| 0 | H | H | L | L | L | L | H | H | H | H | H | H | H | L | 1 |
| 1 | H | X | L | L | L | H | H | L | H | H | L | L | L | L | |
| 2 | H | X | L | L | H | L | H | H | H | L | H | H | L | H | |
| 3 | H | X | L | L | H | H | H | H | H | H | H | L | L | H | |
| 4 | H | X | L | H | L | L | H | L | H | H | L | L | H | H | |
| 5 | H | X | L | H | L | H | H | H | L | H | H | L | H | H | |
| 6 | H | X | L | H | H | L | H | L | L | H | H | H | H | H | |
| 7 | H | X | L | H | H | H | H | H | H | H | L | L | L | L | |
| 8 | H | X | H | L | L | L | H | H | H | H | H | H | H | H | |
| 9 | H | X | H | L | L | H | H | H | H | H | L | L | H | H | |
| 10 | H | X | H | L | H | L | H | L | L | L | H | H | L | H | |
| 11 | H | X | H | L | H | H | H | L | L | H | H | L | L | H | |
| 12 | H | X | H | H | L | L | H | L | H | L | L | L | H | H | |
| 13 | H | X | H | H | L | H | H | H | L | L | H | L | H | H | |
| 14 | H | X | H | H | H | L | H | L | L | L | H | H | H | H | |
| 15 | H | X | H | H | H | H | H | L | L | L | L | L | L | L | |
| BI | X | X | X | X | X | X | L | L | L | L | L | L | L | L | 2 |
| RBI | H | L | L | L | L | L | L | L | L | L | L | L | L | L | 3 |
| LT | L | X | X | X | X | X | H | H | H | H | H | H | H | H | 4 |

H; high level, L; low level, X, irrelevant

- Notes:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
 2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
 3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
 4. When a blanking input / ripple blanking output (BI / RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.



Block Diagram



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---------------------|----------|-------------|------|
| Supply voltage | V_{CC} | 7 | V |
| Input voltage | V_{IN} | 7 | V |
| Power dissipation | P_T | 400 | mW |
| Storage temperature | Tstg | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit |
|-----------------------|-------------------|------|------|------|---------|
| Supply voltage | V_{CC} | 4.75 | 5.00 | 5.25 | V |
| Output current | I_{OH} (a to g) | — | — | -100 | μA |
| | I_{OH} (BI/RBO) | — | — | -50 | μA |
| Output current | I_{OL} (a to g) | — | — | 6 | mA |
| | I_{OL} (BI/RBO) | — | — | 3.2 | mA |
| Operating temperature | T_{opr} | -20 | 25 | 75 | °C |

Electrical Characteristics

(Ta = -20 to +75 °C)

| Item | Symbol | min. | typ.* | max. | Unit | Condition | |
|------------------------------|-----------------|-----------------|-------|------|------|-----------|---|
| Input voltage | V _{IH} | 2.0 | — | — | V | | |
| | V _{IL} | — | — | 0.8 | V | | |
| Output voltage | a to g | V _{OH} | 2.4 | — | — | V | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V |
| | BI / RBO | | 2.4 | — | — | V | |
| | a to g | V _{OL} | — | — | 0.4 | V | V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V |
| | | | — | — | 0.5 | V | |
| | BI / RBO | | — | — | 0.4 | V | |
| | | | — | — | 0.5 | V | |
| Output current** | a to g | I _O | -1.3 | — | — | mA | V _{CC} = 4.75 V, V _O = 0.85 V, |
| Input current | except BI / RBO | I _{IH} | — | — | 20 | μA | V _{CC} = 5.25 V, V _I = 2.7 V |
| | | I _{IL} | — | — | -0.4 | mA | V _{CC} = 5.25 V, V _I = 0.4 V |
| | BI / RBO | I _I | — | — | -1.2 | mA | V _{CC} = 5.25 V, V _I = 0.4 V |
| Short-circuit output current | BI / RBO | I _{OS} | — | — | 0.1 | mA | V _{CC} = 5.25 V, V _I = 7 V |
| | | | — | — | -2 | mA | V _{CC} = 5.25 V |
| Supply current*** | | I _{CC} | — | 25 | 38 | mA | V _{CC} = 5.25 V |
| Input clamp voltage | | V _{IK} | — | — | -1.5 | V | V _{CC} = 4.75 V, I _{IN} = -18 mA |

Notes: * V_{CC} = 5 V, Ta = 25°C

** Input condition as for V_{OH}

*** I_{CC} is measured with all outputs open and inputs at 4.5 V.

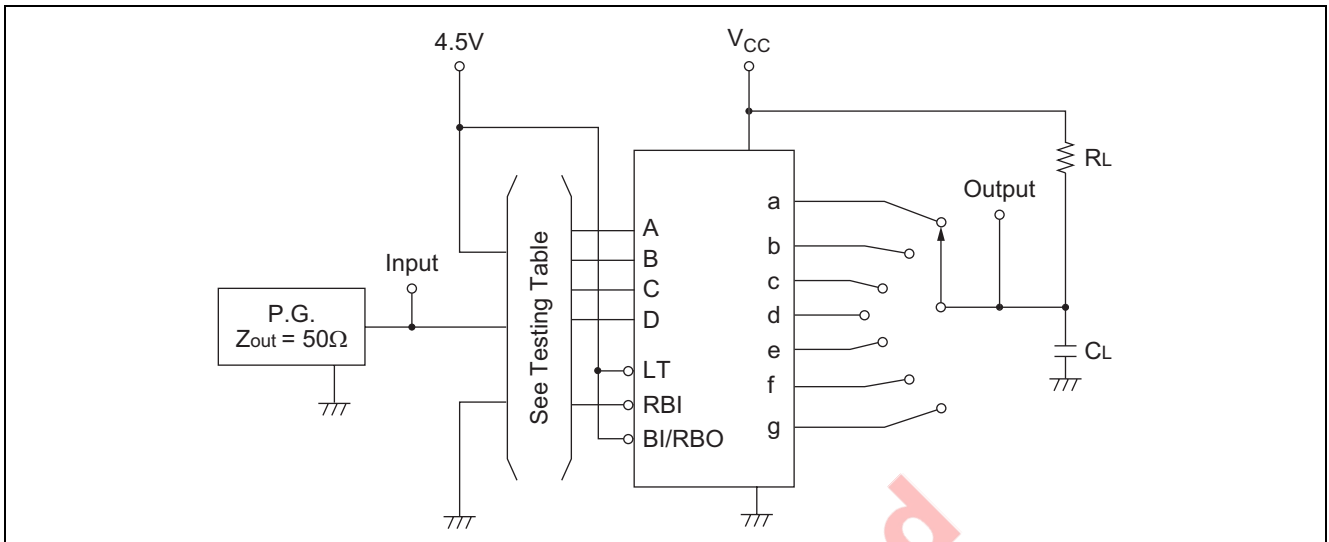
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

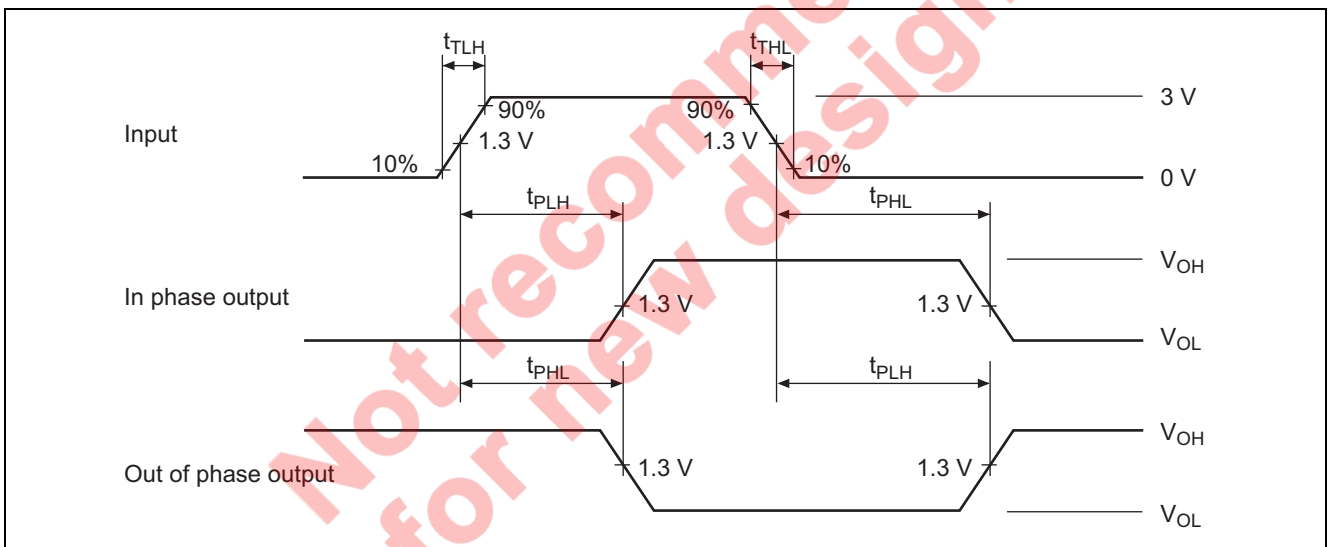
| Item | Symbol | Input | min. | typ. | max. | Unit | Condition |
|---------------|------------------|-------|------|------|------|------|---|
| Turn-on time | t _{PHL} | A | — | — | 100 | ns | C _L = 15 pF, R _L = 4 kΩ |
| | t _{PLH} | | — | — | 100 | | |
| Turn-off time | t _{PHL} | RBI | — | — | 100 | ns | C _L = 15 pF, R _L = 6 kΩ |
| | t _{PLH} | | — | — | 100 | | |

Testing Method

Test Circuit



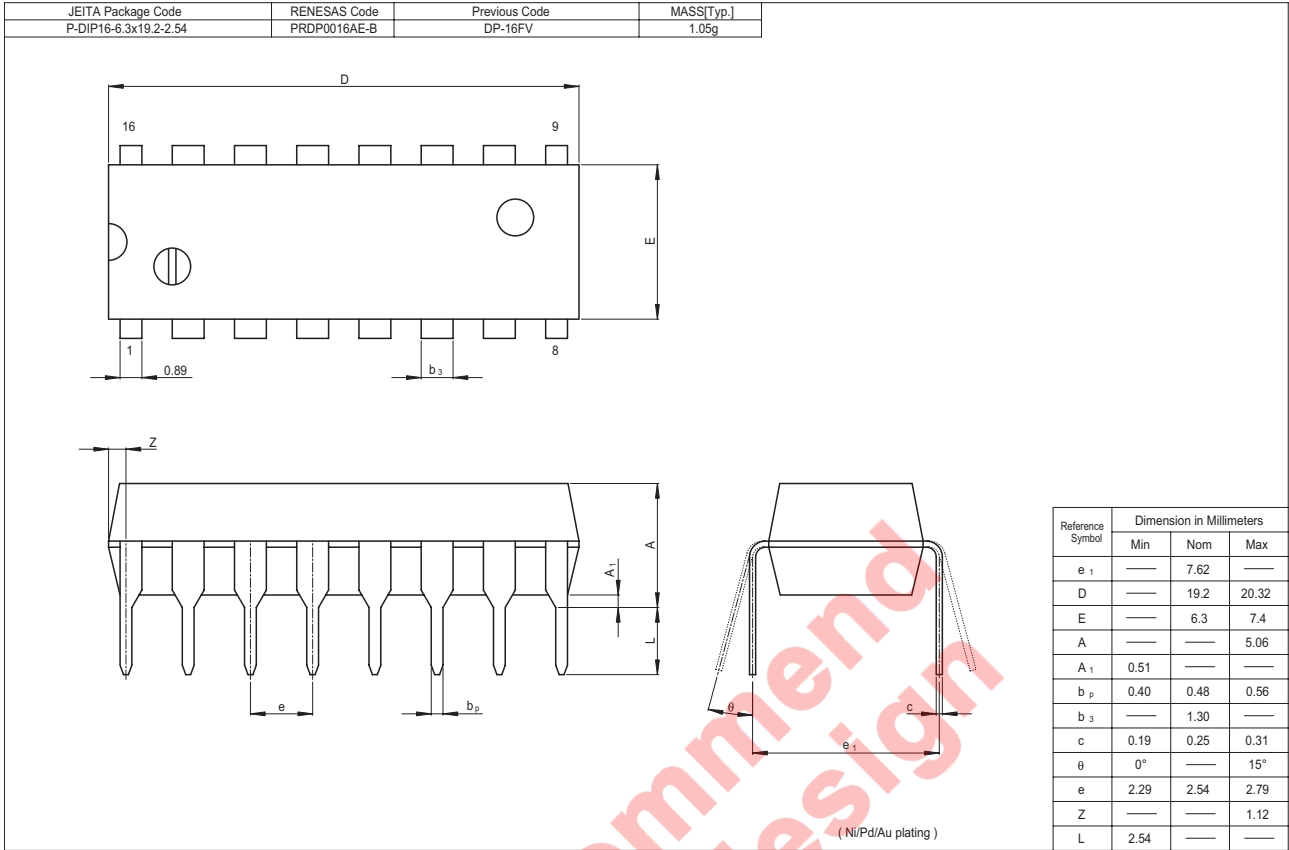
Waveform



Testing Table

| Item | Inputs | | | | | Outputs | | | | | | |
|--------------------------------------|--------|-----|-------|-------|-----|---------|-----|-----|-----|-----|-----|-----|
| | RBI | D | C | B | A | a | b | c | d | e | f | g |
| t _{PLH} t _{PHL} | 4.5 V | GND | GND | GND | IN | OUT | — | — | OUT | OUT | OUT | — |
| | 4.5 V | GND | GND | 4.5 V | IN | — | — | OUT | — | OUT | — | — |
| | 4.5 V | GND | 4.5 V | 4.5 V | IN | OUT | OUT | — | OUT | OUT | OUT | OUT |
| | IN | GND | GND | GND | GND | OUT | OUT | OUT | OUT | OUT | OUT | — |

Package Dimensions



Not recommended for new design

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510